Single chip 2.4 GHz Transceiver with Embedded ANT protocol

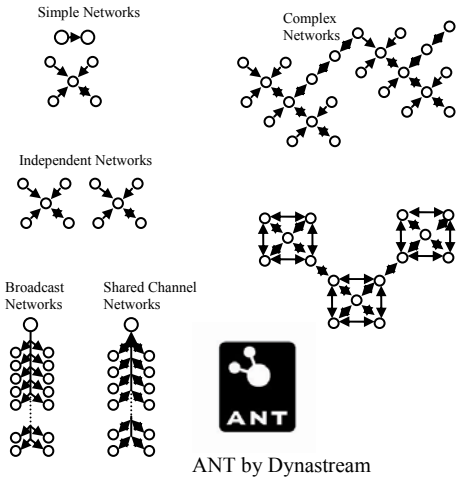
nRF24AP1

FEATURES

- Integrated PAN (Personal Area Network)
- Drop in wireless networking with simple serial interface
- 2.4GHz Worldwide ISM Band
- Ultra-low power (coin cell battery)
- Fully scaleable
- Broadcast, Acknowledged or Burst Data
- Message rates 0.5Hz -> 200Hz (8byte data payload)
- Burst transfer rates up to 20kbps (true data throughput)
- Public and private networks
- 1 Mbps RF data rate
- 125 RF channels

APPLICATIONS

- Sensor Networks
- Industrial Automation
- Home Automation
- Sports Monitoring



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GENERAL DESCRIPTION

The nRF24AP1 is an ultra-low power single-chip radio transceiver with embedded ANT protocol for personal area networks. The transceiver's RF operating frequency range falls within the world-wide 2.4 - 2.5 GHz RF ISM band, allowing for regulatory compliance and product sales into global markets.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum data rate (over the air)	1000	kbps
Temperature range	-40 to +85	°C
Sensitivity	-80	dBm
Average current consumption as low as	30	µA
Peak current consumption TX @-5dBm	13.5mA for 350us	mA
Peak current consumption RX	22mA for 600us	mA
Max # of simultaneous connections[1]	>65000	connections
Max # of simultaneous independent 2-way connections	4	2-way connections
Maximum sustained transfer rate (all data – no overhead)[2]	20	kbps
CR2032 Battery life in a typical sensor application[3]	5	years

Table 1: nRF24AP1 quick reference data

[1] Using Shared Channel Network
[2] Transfer rate refers to data rate of the end application's message payload
[3] Message interval of 2s, 1 hour/day usage



The transceiver consists of the ANT fully integrated protocol engine, frequency synthesizer, power amplifier, crystal oscillator and modulator, and can be interfaced to a host micro controller over either a synchronous or asynchronous serial interface. Designed to run on a wrist-watch coin cell battery, current consumption of the device is extremely low - a typical sensor application can operate on approximately 30µA average current consumption. Short, low peak current transitions are battery friendly.

The embedded ANT protocol makes for easy, low cost integration. Eliminating the need for 3rd party RF protocol implementation, the on-chip ANT protocol combined with the 2.4GHz transceiver enables system and application developers to interact with the nRF24AP1 as a black box wireless solution. The simple serial interface (asynchronous or synchronous) to the device allows for flexibility and scalability from ultra-low power sensors (30µA) through to higher data rate (20kbps) applications implemented in a multitude of network configurations. Networks can be scaled from as little as two nodes to thousands. With 2^{32} unique IDs, multiple radio frequencies, public and private network management and scalable data rates, an unlimited number of network configurations and applications are possible.

Prior to reading this document, the "ANT Message Protocol and Usage" document should be read to gain understanding of the ANT protocol capabilities.

REFERENCES

Ref. No.	Doc. No.	Revision	Title
1	D00000794	1.0	Interfacing with ANT General Purpose Chipset and Modules (Part of nRF24AP1 Specification)
2	D00000652	1.36	ANT Message Protocol and Usage

Table 2 nRF24AP1 referenced documents

For more information see: www.nordicsemi.no

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1. BLOCK DIAGRAM

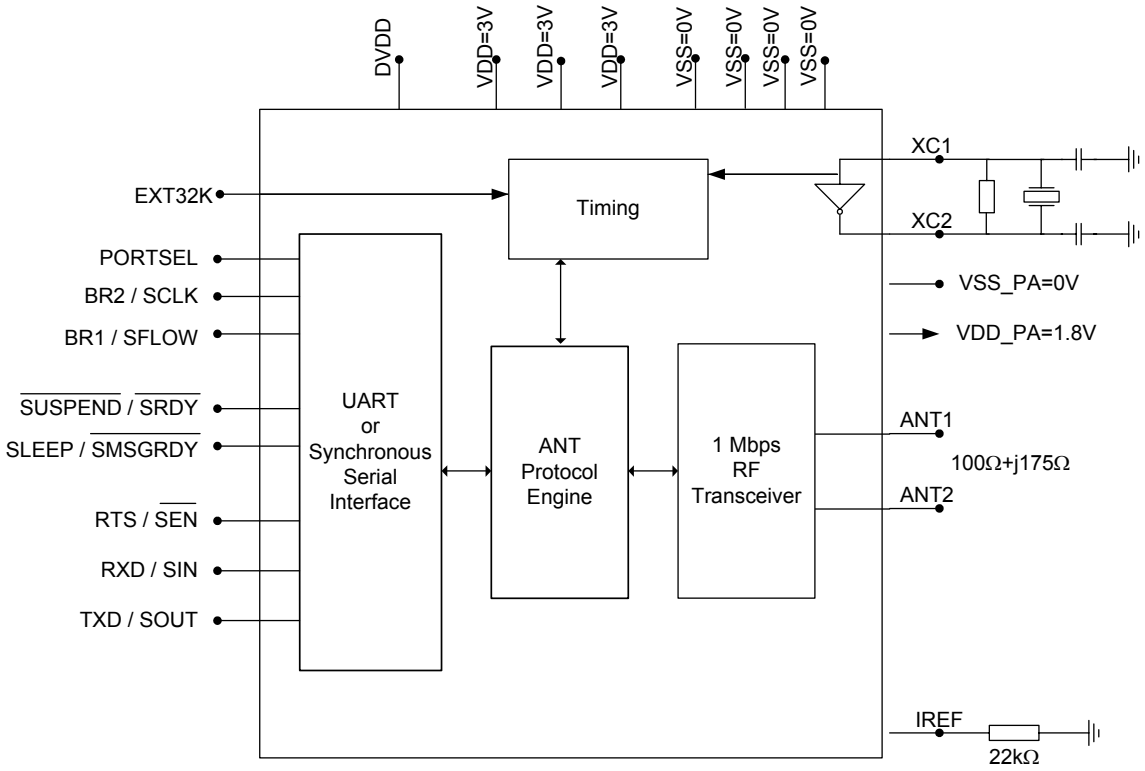


Figure 1: nRF24AP1 with external components.

The “ANT Protocol Engine” shown in Figure 1 is described in the “ANT Message Protocol and Usage” document.

2. PIN FUNCTIONS

Pin	Name	Pin function	Description
1	BR2 / SCLK	Digital IO	Asynchronous baud rate select / Synchronous clock signal
2	BR1 / SFLOW	Digital Input	Asynchronous baud rate select / Synch. Bit or byte flow select
3	EXT32K	Digital Input	Optional External 32kHz clock, tied to GND when not used
4	RXD / SIN	Digital Input	Asynchronous UART receive data / Synchronous receive data
5	TXD / SOUT	Digital Output	Asynchronous UART transmit data / Synchronous transmit data
6	SLEEP / $\overline{\text{SMSGRDY}}$	Digital Input	Asynchronous sleep enable / Synchronous message ready signal
7	$\overline{\text{SUSPEND}}$ / $\overline{\text{SRDY}}$	Digital Input	Asynchronous suspend control / Synchronous port ready signal
8	RTS / $\overline{\text{SEN}}$	Digital Output	Asynchronous flow control RTS /Synchronous serial enable
9	DVDD	Power Output	Positive Digital Supply output for de-coupling purposes
10	VSS	Power	Ground (0V)
11	XC2	Analog Output	Crystal Pin 2
12	XC1	Analog Input	Crystal Pin 1
13	VDD_PA	Power Output	Power Supply (+1.8V) to Power Amplifier
14	ANT1	RF	Antenna interface 1
15	ANT2	RF	Antenna interface 2
16	VSS_PA	Power	Ground (0V)
17	VDD	Power	Power Supply (+3V DC)
18	VSS	Power	Ground (0V)
19	IREF	Analog Input	Reference current
20	VSS	Power	Ground (0V)
21	VDD	Power	Power Supply (+3V DC)
22	VSS	Power	Ground (0V)
23	PORTSEL	Digital Input	Asynchronous / Synchronous port selection
24	VDD	Power	Power Supply (+3V DC)

Table 3: nRF24AP1 pin function

3. PIN ASSIGNMENT

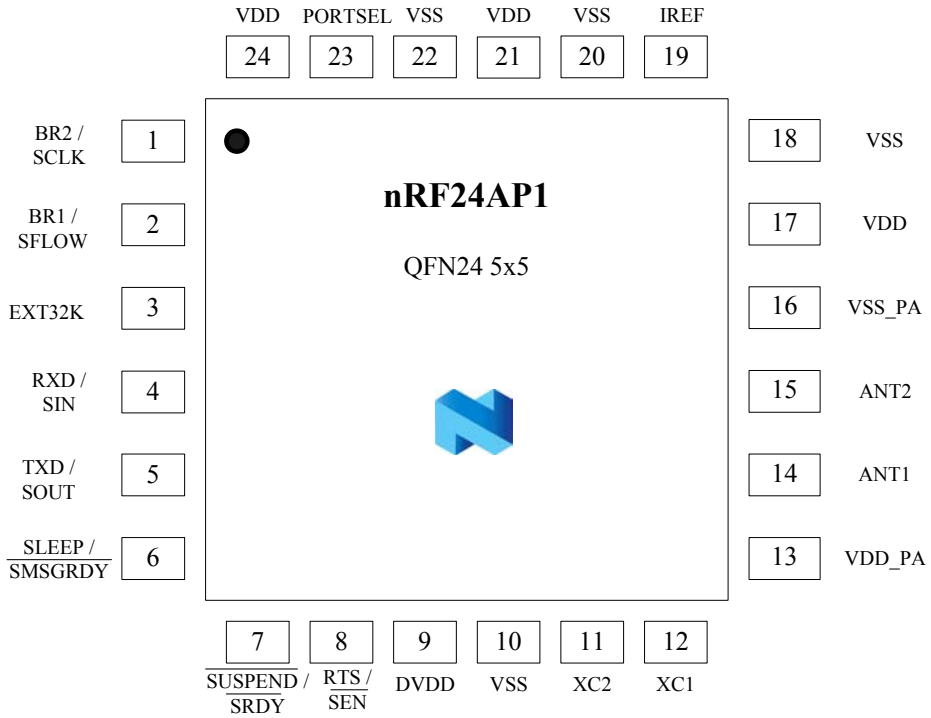


Figure 2: nRF24AP1 pin assignment (top view) for a QFN24 5x5 package.

4. ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, TA = - 40ºC to + 85ºC

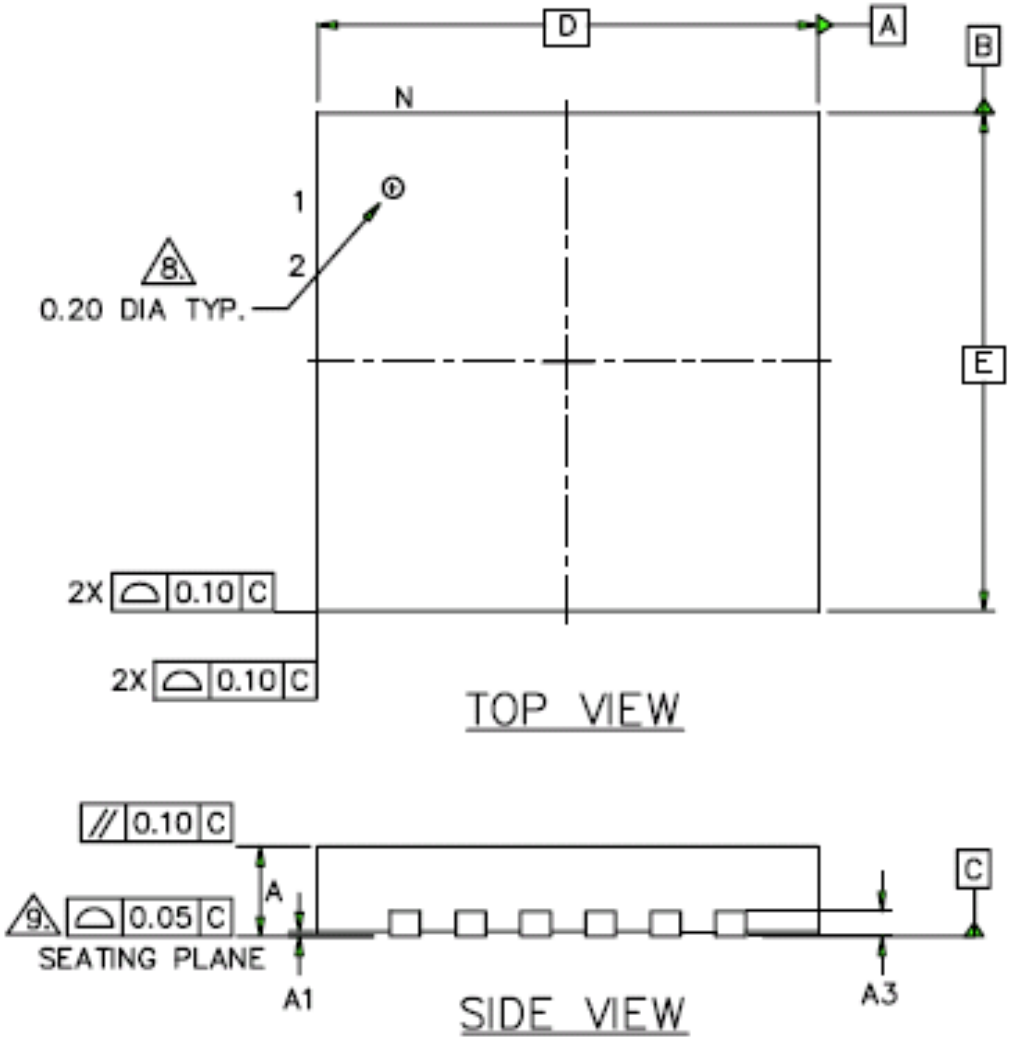
Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Operating conditions					
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		0.7VDD		VDD	V
V_{IL}	LOW level input voltage		VSS		0.3VDD	V
	Digital output pin					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD- 0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		VSS		0.3	V
	Crystals and clocks					
f_{XTAL}	RF Crystal frequency			16		MHz
$f_{XTAL-OFFSET}$	RF Crystal offset (Initial, Temp & Aging)				30	PPM
f_{EXT32K}	EXT32K – external 32.768kHz clock			32.768		kHz
$f_{EXT32K-ERROR}$	Maximum error for 32.768kHz clock				50	PPM
	Synchronous Serial Timing					
sclk freq.	Synchronous clock frequency (byte mode)			150-175		kHz
$t_{ReadValid}$	Data is valid on read before low to high transition on the clock (byte mode)		0.5			µs
$t_{WriteValid}$	Data must be valid on write within this time after a high to low transition on the clock (byte mode)				2	µs
t_{SRDY_MinLow}	Minimum $\overline{\text{SRDY}}$ low time		2.5			µs
t_{Reset}	Synchronous Reset. $\overline{\text{SRDY}}$ falling edge to $\overline{\text{SMSGRDY}}$ falling edge		250			µs
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2524	MHz
$F_{CHANNEL}$	Channel spacing			1		MHz
Δf	Frequency deviation			±156		kHz
	Current Consumption					
I_{Idle}	No active channels – No communications			2		µA
I_{Peak}	Peak Current consumption, RX	2)		22		mA
I_{PeakTX}	Peak Current – TX @ 0dBm	3)		16		mA
	Transmitter operation					
P_{RF}	Maximum Output Power	4)		0	+4	dBm
P_{RFC}	RF Power Control Range		16	20		dB
P_{RFCR}	RF Power Control Range Resolution				±3	dB
P_{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P_{RF2}	2nd Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF3}	3rd Adjacent Channel Transmit Power 3MHz				-40	dBm
I_{VDD}	Supply peak current @ 0dBm output power	4)		16		mA
I_{VDD}	Supply peak current @ -20dBm output power	4)		13		mA
	Receiver operation					
I_{VDD}	Supply peak current receive mode	4)		22		mA
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-80		dBm
C/I_{CO}	C/I Co-channel			10/4		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			-20/0		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-37/-20		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-43/-30		dB

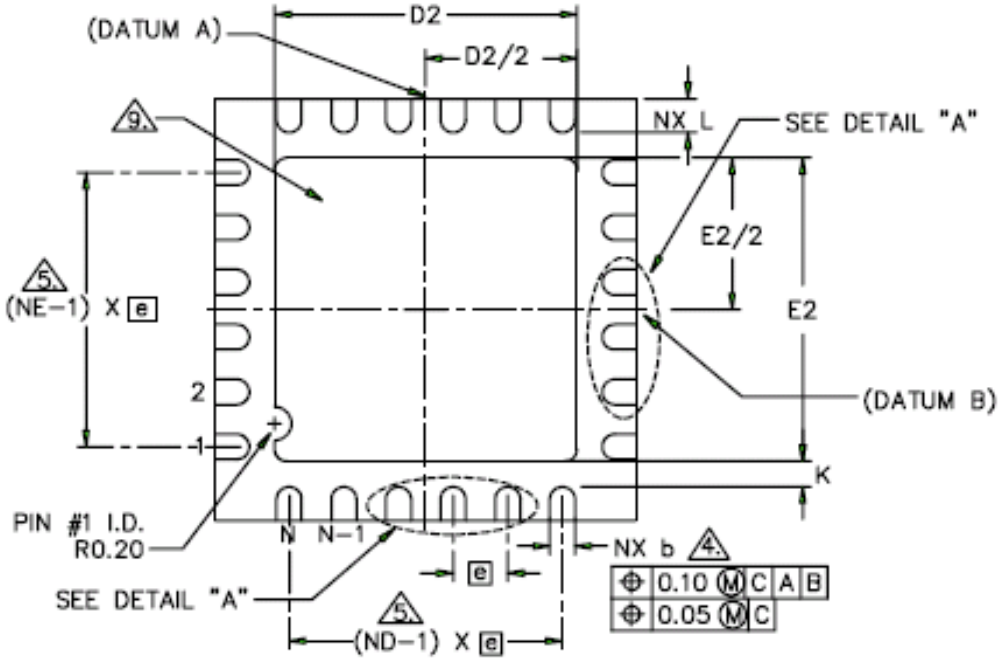
1) Usable band is determined by local regulations
2) Time of Maximum Current consumption in RX is typical 600us and maximum 1ms
3) Time of Maximum TX Only Current is typical 400us and maximum 400us.
4) Antenna load impedance = 100Ω+j175Ω

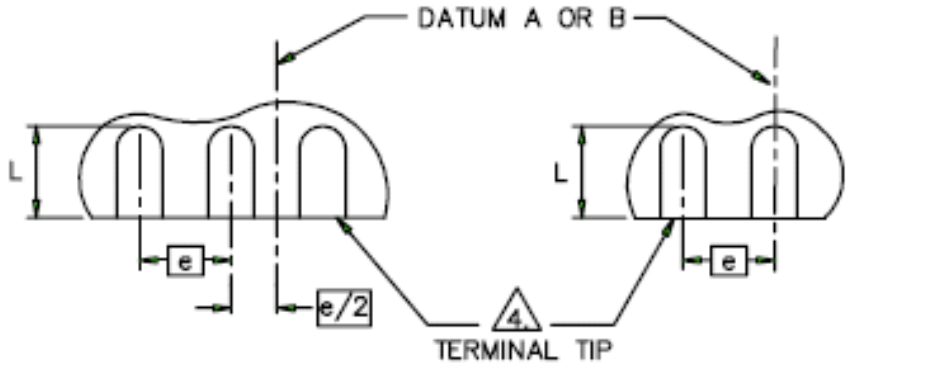
Table 4: nRF24AP1 RF specifications

5. PACKAGE OUTLINE

nRF24AP1 uses the QFN24 5x5 package, with matt tin plating.







Package Type		A	A1	A3	K	D/E	e	D2/E2	L	b
SAW	**Min**	0.8	0.00	0.20	0.20	5.0	0.65	3.50	0.35	0.25
QFN24 (5x5)	**Typ**	0.85	0.02	REF.	MIN.	BSC	BSC	3.60	0.40	0.30
	Max	0.90	0.05					3.70	0.45	0.35

Figure 3 nRF24AP1 package outline.



5.1 Package marking:

n	R	F		*B*	*X*
2	4	A	P	1	
Y	*Y*	*W*	*W*	*L*	*L*

Abbreviations:

B – Build Code, i.e. unique code for production sites, package type and test platform
X – "X" grade, i.e. Engineering Samples (optional)
YY – 2 digit Year number
WW – 2 digit Week number
LL – 2 letter wafer lot number code

6. ORDERING INFORMATION

Ordering code	Description	Package	Container	MOQ[4]
nRF24AP1-REEL	1 Mbps Transmitter	24 pin QFN 5x5	Tape and reel[5]	4000
nRF24AP1-REEL7	1 Mbps Transmitter	24 pin QFN 5x5	Tape and reel[5]	1500
nRF24AP1	1 Mbps Transmitter	24 pin QFN 5x5	Tray	490
nRF24AP1-EVKIT	4 node evaluation and development kit	N/A	N/A	1

Table 5 nRF24AP1 ordering information

[4] MOQ = Minimum order quantity
[5] **Moisture Sensitivity Level:** MSL2@260ºC, three times reflow

7. ABSOLUTE MAXIMUM RATINGS

Supply voltages
VDD ..... - 0.3V to + 3.6V
VSS 0V

Input voltage
V_I ..... - 0.3V to VDD + 0.3V

Output voltage
V_O ..... - 0.3V to VDD

Total Power Dissipation
P_D (T_A=85°C) 90mW

Temperatures
Operating Temperature…. - 40°C to + 85°C
Storage Temperature……. - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic Sensitive Device
Observe Precaution for handling.





Glossary of Terms

Term	Description
Acknowledged Data	Data for which the transmitter receives an acknowledgement from the receiver
ANT	Ultra-low power embedded RF protocol
Broadcast Data	Default transmission type. Data sent on every time slot
Burst Data	Bulk data transmission between two nodes
Channel	Basic building block of ANT. Connects two devices together
Device ID	Device ID – Identifier for the master end of the channel
Device Number	Device Number is a subcomponent of Device ID, uniquely identifying this device
Device Type	Device Type is a subcomponent of Device ID, uniquely identifying the type of this device
Forward Channel	Data transmission from Master to Slave on a channel
GFSK	Gaussian Frequency Shift Keying
HOST MCU	The MCU which interfaces and controls the nRF24AP1
ISM	Industrial-Scientific-Medical
ISM Band	Industrial, Scientific and Medical Band
Manufacturer ID	Manufacturer ID is a subcomponent of Device ID, uniquely identifying the manufacturer of this device
Master	Primary transmitter of the ANT network channel
MCU	Micro controller unit
Message Data rate	Number of messages per second sent over a channel
Message Payload	User portion of a data packet. Each data packet contains a payload of 8 bytes.
Message	Data packet sent over a channel from one device to another
Networks	A group of ANT nodes connected together via channels forms a network in which the nodes may communicate with one another
Node	An application running on a host controller connected to an nRF24AP1, which communicates with other ANT nodes.
Pairing	The process in which a Slave obtains the Master's ID in order to establish communications.
Reverse Channel	Data transmission from Slave to Master on a channel
RF data rate	The on air data rate. This rate is 1Mbps.
RF Frequency	RF Frequency used for communications. The nRF24AP1 can be configured to one of 125 different RF frequencies.
RX	Receive
Slave	Primary receiver of the ANT network channel
TX	Transmit

Table 6: Glossary



8. ARCHITECTURAL OVERVIEW

The nRF24AP1 is a single-chip silicon solution that integrates a 2.4GHz transceiver and the ANT RF protocol stack. The ANT protocol stack is stored on-chip and is executed by the nRF24AP1's internal MCU core.

Functionally, the nRF24AP1 is composed of 4 main building blocks as shown in Figure 1. Together, the 4 blocks enable the drop-in RF and protocol solution. As shown, the 4 main blocks are the serial interface, the timing interface, the ANT protocol engine, and the RF transceiver. Both the ANT protocol engine and the RF transceiver are embedded within the device and interact with the external host environment through a UART or synchronous serial interface. This functional approach allows the nRF24AP1 to be treated as a black box wireless solution from the system application perspective. Integration of an RF protocol with the RF physical layer is not required. Application developers provides channel configuration and message data information to the device through the serial interface, and the nRF24AP1 executes the configuration and sends/receives the message data packets over the air to other waiting devices.

ANT is a 2.4GHz bidirectional wireless Personal Area Network (PAN) communications technology optimized for transferring low data-rate, low latency data between multiple ANT-enabled devices. The ultra-low power consumption of ANT guarantees an extended battery life even from low capacity supplies such as a coin cell battery, such as are required for heart rate monitors, bicycle computers, and wrist watches. The small size and low-cost implementation of ANT proves essential in allowing effortless integration into the tiny form factor of wrist watches, PDAs, and mobile phones.

The ANT – HOST interface has been designed with utmost simplicity in mind so that it can be easily and quickly implemented into new devices and applications. The encapsulation of the wireless protocol complexity within the ANT chipset vastly reduces the burden on the application host controller, allowing a low-cost 4-bit or 8-bit Microcontroller (MCU) to establish and maintain complex wireless networks with remote devices. Data transfers can be scheduled in a deterministic or ad-hoc fashion, and a burst mode allows for the efficient transfer of large amounts of stored data to and from a PC or other computing device. The ANT system aggressively balances functionality, cost, size, and power consumption within the constraints of a mobile Personal Area Network.

The ANT protocol implements layers 1-4 of the OSI networking stack as well as automatically providing session authentication of network devices. For description of layer 3 and 4, please refer to the "ANT Message Protocol and Usage" document.



9. ANT INTERFACE

9.1 Physical Layer – Serial Interfacing

The ANT serial interface between host controller and nRF24AP1 can be implemented over either a synchronous or asynchronous connection, which can be selected by the product developer as preferred for a given implementation. The precise details of the physical connections and signaling can be found in the 'Interfacing with ANT General Purpose Chipsets and Modules' document.

9.2 ANT Message Summary

The table in Section 9.4 summarizes the message types employed between the host controller and the nRF24AP1, which are used to establish and maintain RF connections to remote devices. Further details of the message fields and data contents can be found in the 'ANT Message Protocol and Usage' document.

9.3 32kHz Clock Signal (EXT32K)

A 32.768kHz clock signal may optionally be provided to the nRF24AP1. If this signal is not used, it must be connected to ground. Please see the electrical specification section for external clock specifications. Use of an external clock is recommended for power sensitive applications. The nRF24AP1 automatically detects the presence of an external clock source upon power up. In order to avoid timing issues between when the external clock source becomes present, and when the nRF24AP1 samples for this signal, it is recommended that a SystemReset (see Message Summary table below) command is issued to the nRF24AP1 upon initial connection. This will ensure that the external clock is properly detected and used. Once the EXT32K signal has been provided on power up it must remain present as long as the nRF24AP1 remains powered up.



9.4 Message Summary

Class	Type	ANT PC Interface Function	Response	From	Len	Msg ID	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Data 8	Data 9
Channel Event Messages	Channel Response / Event	->ChannelEventFunc(Chan, MessageCode) or ->ResponseFunc(Chan, MsgID);	-	ANT	3	0x40	Channel Number	Message ID	Message Code						
Requested Response Messages	Channel Status	->ResponseFunc(Chan,0x52)	-	ANT	2	0x52	Channel Number	Channel Status							
	Channel ID	->ResponseFunc(Chan,0x51)	-	ANT	5	0x51	Channel Number	Device Number		Device Type ID	Man ID				
	ANT Version	->ResponseFunc(-, 0x3D)	-	ANT	9	0x3D	Ver0	Ver1	Ver2	Ver3	Ver4	Ver5	Ver6	Ver7	Ver8
	Capabilities	->ResponseFunc(-, 0x54)	-	ANT	4	0x54	Max Channels	Max Networks	Standard Options	Advanced Options					
Config. Messages	Unassign Channel	ANT_UnAssignChannel()	Yes	HOST	1	0x41	Channel Number								
	Assign Channel	ANT_AssignChannel()	Yes	HOST	3	0x42	Channel Number	Channel Type	Network Number						
	Channel ID	ANT_SetChannelID()	Yes	HOST	5	0x51	Channel Number	Device Number		Device Type ID	Man ID				
	Channel Period	ANT_SetChannelPeriod()	Yes	HOST	3	0x43	Channel Number	Messaging Period							
	Search Timeout	ANT_SetChannelSearchTimeout()	Yes	HOST	2	0x44	Channel Number	Search Timeout							
	Channel RF Frequency	ANT_SetChannelRFFreq()	Yes	HOST	2	0x45	Channel Number	RF Frequency							
	Set Network	ANT_SetNetworkKey()	Yes	HOST	9	0x46	Net #	Key 0	Key 1	Key 2	Key 3	Key 4	Key 5	Key 6	Key 7
	Transmit Power	ANT_SetTransmitPower()	Yes	HOST	2	0x47	0	TX Power							
Test Mode	CW Init	ANT_InitCWTestMode()	Yes	HOST	1	0x53	0								
	CW Test	ANT_SetCWTestMode()	Yes	HOST	3	0x48	0	TX Power	RF Freq						
Control Messages	SystemReset	ANT_ResetSystem()	No	HOST	1	0x4A	0								
	Open Channel	ANT_OpenChannel()	Yes	HOST	1	0x4B	Channel Number								
	Close Channel	ANT_CloseChannel()	Yes	HOST	1	0x4C	Channel Number								
	Request Message	ANT_RequestMessage()	Yes	HOST	2	0x4D	Channel Number	Message ID							
Data Messages	Broadcast Data	ANT_SendBroadcastData() ->ChannelEventFunc(Chan, EV)	No	ANT/ HOST	9	0x4E	Channel Number	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
	Acknowledge Data	ANT_SendAcknowledgedData() ->ChannelEventFunc(Chan, EV)	No	ANT/ HOST	9	0x4F	Channel Number	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
	Burst Transfer Data	ANT_SendBurstTransferPacket() ->ChannelEventFunc(Chan, EV)	No	ANT/ HOST	9	0x50	Sequence/ Channel Number	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7



10. APPLICATION SPECIFIC CURRENT CONSUMPTION

Symbol	Parameter (condition)	Typ.	Units
I_{Idle}	No active channels – No communications	2	µA
$I_{Suspend}$	Asynchronous suspend Activated	2	µA
$I_{Base-Ext}$	Active base current when EXT32K used	35	µA
$I_{Base-Int}$	Active base current with no EXT32K	75	µA
I_{Peak}	Peak Current consumption, RX	22	mA
I_{PeakTX}	Peak Current – TX @ 0dBm	16	mA
$I_{RX_ByteSync}$	Average Current / RX message byte sync	19	µA
$I_{RX_BitSync}$	Average Current / RX message bit sync	29	µA
I_{RX_50k}	Average Current / RX message 50Kbaud async	21	µA
$I_{RX_38.4k}$	Average Current / RX message 38.4Kbaud async	24	µA
$I_{RX_19.2k}$	Average Current / RX message 19.2Kbaud async	32	µA
I_{RX_4800}	Average Current / RX message 4800baud async	85	µA
$I_{TX_ByteSync}$	Average Current / TX message byte sync	11	µA
$I_{TX_BitSync}$	Average Current / TX message bit sync	26	µA
I_{TX_50k}	Average Current / TX message 50Kbaud async	19	µA
$I_{TX_38.4k}$	Average Current / TX message 38.4Kbaud async	21	µA
$I_{TX_19.2k}$	Average Current / TX message 19.2Kbaud async	37	µA
I_{TX_4800}	Average Current / TX message 4800baud async	119	µA
$I_{TR_ByteSync}$	Average Current / bi-directional TX message byte sync	26	µA
$I_{TR_BitSync}$	Average Current / bi-directional TX message bit sync	38	µA
I_{TR_50k}	Average Current / bi-directional TX message 50Kbaud async	33	µA
$I_{TR_38.4k}$	Average Current / bi-directional TX message 38.4Kbaud async	35	µA
$I_{TR_19.2k}$	Average Current / bi-directional TX message 19.2Kbaud async	49	µA
I_{TR_4800}	Average Current / bi-directional TX message 4800baud async	131	µA
$I_{ARX_ByteSync}$	Average Current / Acknowledged RX message byte sync	28	µA
$I_{ARX_BitSync}$	Average Current / Acknowledged RX message bit sync	51	µA
I_{ARX_50k}	Average Current / Acknowledged RX message 50Kbaud async	38	µA
$I_{ARX_38.4k}$	Average Current / Acknowledged RX message 38.4Kbaud async	42	µA
$I_{ARX_19.2k}$	Average Current / Acknowledged RX message 19.2Kbaud async	48	µA
I_{ARX_4800}	Average Current / Acknowledged RX message 4800baud async	102	µA
$I_{ATX_ByteSync}$	Average Current / Acknowledged TX message byte sync	37	µA
$I_{ATX_BitSync}$	Average Current / Acknowledged TX message bit sync	55	µA
I_{ATX_50k}	Average Current / Acknowledged TX message 50Kbaud async	47	µA
$I_{ATX_38.4k}$	Average Current / Acknowledged TX message 38.4Kbaud async	50	µA
$I_{ATX_19.2k}$	Average Current / Acknowledged TX message 19.2Kbaud async	70	µA
I_{ATX_4800}	Average Current / Acknowledged TX message 4800baud async	146	µA
I_{Ave}	Broadcast TX@ 0.5Hz byte sync,EXT32K	30	µA
I_{Ave}	Broadcast TX @ 2 Hz byte sync,EXT32K	52	µA
I_{Ave}	Broadcast RX @ 0.5Hz byte sync,EXT32K	34	µA
I_{Ave}	Acknowledged TX@ 0.5 Hz byte sync,EXT32K	43	µA
I_{Ave}	Acknowledged RX@ 0.5 Hz byte sync,EXT32K	38	µA
I_{Ave}	Burst continuous @ 20 kbps, byte synchronous	4.92	mA
I_{Ave}	Burst continuous @ 7.5 kbps, bit synchronous	5.7	mA
I_{Ave}	Burst continuous @ 20 kbps, asynchronous (50k)	5.4	mA
I_{Ave}	Burst continuous @ 13. kbps, asynchronous (38.4k)	5.5	mA
I_{Ave}	Burst continuous @ 8.5 kbps, asynchronous (19.2k)	5.85	mA

Table 7: Application specific current consumption

11. PERIPHERAL RF INFORMATION

11.1 Antenna output

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD, either via a RF choke or via the center point in a dipole antenna. A load of 100Ω+j175Ω between the ANT1/ANT2 is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network.

11.2 Output Power adjustment

RF output power	Peak current consumption
0 dBm ±3dB	16.0 mA
-5 dBm ±3dB	13.5 mA
-10 dBm ±3dB	12.5 mA
-20 dBm ±3dB	12 mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 100Ω+j175Ω.

Table 8: RF output power setting for the nRF24AP1

11.3 Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance
16	12pF	100 Ω	7.0pF	±50ppm

Table 9: Crystal specification of the nRF24AP1

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying C_L=12pF is OK, but it is possible to use up to 16pF. Specifying a lower value of crystal parallel equivalent capacitance, C_0 will also work, but this can increase the price of the crystal itself. Typically C_0=1.5pF at a crystal specified for C_{0max}=7.0pF.



11.4 Sharing crystal with micro controller

When using a micro controller to drive the crystal reference input XC1 of the nRF24AP1 transceiver some rules must be followed.

11.5 Crystal parameters:

When the micro controller drives the nRF24AP1 clock input, the requirement of load capacitance C_L is set by the micro controller only. The frequency accuracy of ±50 ppm is still required to get a functional radio link. The nRF24AP1 will load the crystal by 0.5pF at XC1 in addition to the PBC routing.

11.6 Input crystal amplitude & Current consumption

The input signal should not have amplitudes exceeding any rail voltage, but any DC-voltage within this is OK. Exceeding rail voltage will excite the ESD structure and the radio performance is degraded below specification. If testing the nRF24AP1 with a RF source with no DC offset as the reference source, the input signal will go below the ground level, which is not acceptable.

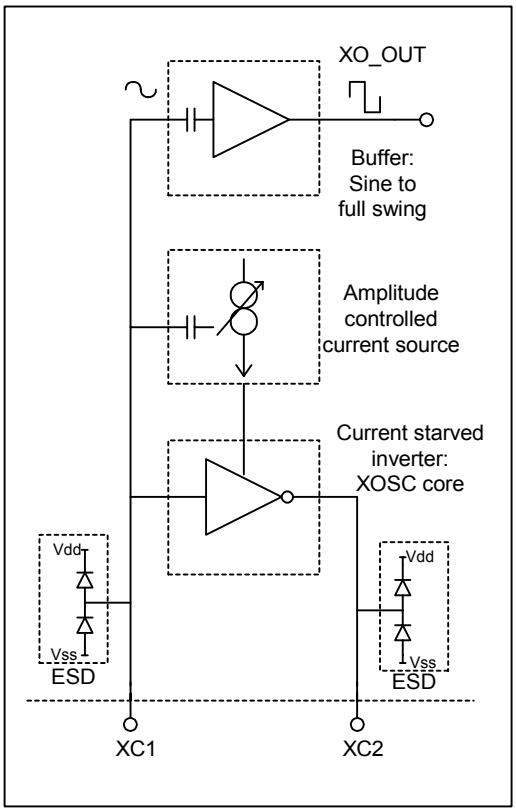


Figure 4: Principle of crystal oscillator

It is recommended to use a DC-block before the XC1 pin so that the internal ESD structures will self bias the XC1 voltage.

The nRF24AP1 crystal oscillator is amplitude regulated. To achieve low current consumption and also good signal-to-noise ratio, it is recommended to use an input signal larger than 0.4 V-peak. The needed input swing is independent of the crystal frequency. When clocking the nRF24AP1 externally, XC2 is not used and can be left as an open pin.



11.7 PCB layout and de-coupling guidelines

A well-designed PCB is necessary to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality, if due care is not taken. A fully qualified RF-layout for the nRF24AP1 and its surrounding components, including matching networks, can be downloaded from **www.nordicsemi.no**.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF24AP1 DC supply voltage should be de-coupled as close as possible to the VDD pins with high performance RF capacitors, see Table 10. It is preferable to mount a large surface mount capacitor (e.g. 4.7µF tantalum) in parallel with the smaller value capacitors. The nRF24AP1 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF24AP1 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. One via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

11.8 Reflow information

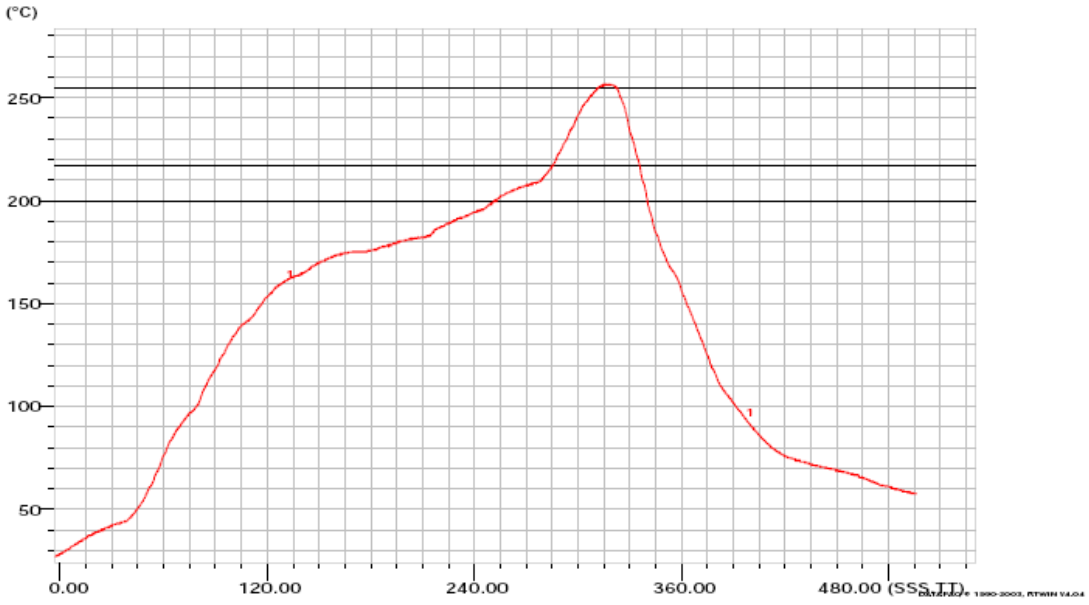


Figure 5 Reflow Soldering profile, GREEN

Ramp rate (RT-150ºC)	1.38 ºC/s
Pre-heat (150-200ºC)	134 s
Dwell @217ºC	50 s
Dwell @245ºC	10 s
Ramp up	1.42 ºC/s
Ramp down	2.59 ºC/s
Peak temperature	257 ºC
Time from RT to PT	320 s

12. APPLICATION EXAMPLE

12.1 nRF24AP1 with single ended matching network

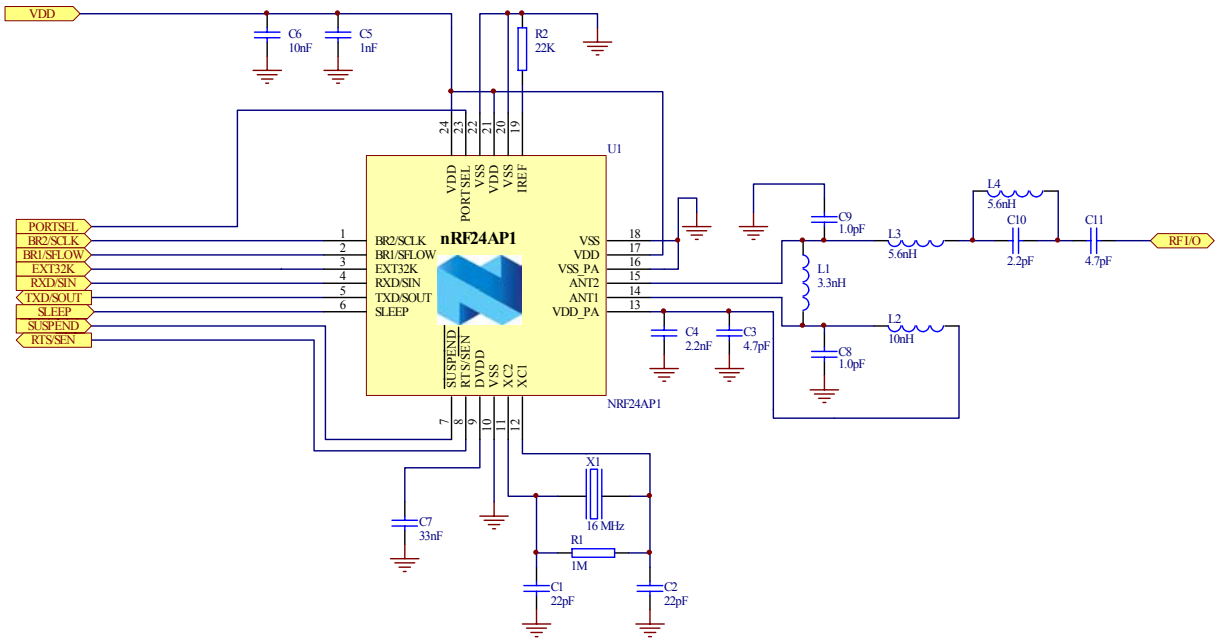


Figure 6: nRF24AP1 schematic for RF layouts with single end 50Ω antenna



Component	Description	Size	Value	Tolerance	Units
C1	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C2	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C3	Capacitor ceramic, 50V, NPO	0603	4.7	±5%	pF
C4	Capacitor ceramic, 50V, X7R	0603	2.2	±10%	nF
C5	Capacitor ceramic, 50V, X7R	0603	1.0	±10%	nF
C6	Capacitor ceramic, 50V, X7R	0603	10	±10%	nF
C7	Capacitor ceramic, 50V, X7R	0603	33	±10%	nF
R1	Resistor	0603	1.0	±10%	MΩ
R2	Resistor	0603	22	±1%	kΩ
U1	nRF24AP1 transceiver	QFN24 / 5x5	nRF24AP1		
X1	Crystal, CL = 12pF, ESR < 100 ohm	LxWxH = 4.0x2.5x0.8	16	+/- 50 ppm	MHz
L1	Inductor	0603	3.3	± 5%	nH
L2	Inductor	0603	10	± 5%	nH
L3	Inductor	0603	5.6	± 5%	nH
L4	Inductor	0603	5.6	± 5%	nH
C8	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.1 pF	pF
C9	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.1 pF	pF
C10	Ceramic capacitor, 50V, NP0	0603	2.2	± 0.25 pF	pF
C11	Ceramic capacitor, 50V, NP0	0603	4.7	± 0.25 pF	pF

Table 10: Recommended components (BOM) in nRF24AP1 with antenna matching network

12.2 PCB layout example

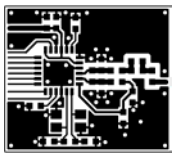
Figure 7 shows a PCB layout example for the application schematic in Figure 6.

A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

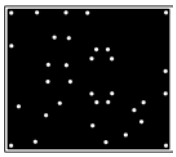


Top silk screen

No components in bottom layer



Top view



Bottom view

Figure 7: nRF24AP1 RF layout with single ended connection to 50Ω antenna and 0603 size passive components



13. DEFINITIONS

Data sheet status	
Objective product specification	This data sheet contains target specifications for product development.
Preliminary product specification	This data sheet contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This data sheet contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 11: Definitions

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Preliminary Product Specification: Revision Date: 05.09.2006.

Data sheet order code: 050906-nRF24AP1

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